BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Miller on edge

The last installment of Analog Domain derived the value for the Miller capacitance—the effective impedance between the collector and the base of a bipolar transistor in a common-emitter configuration (**Reference 1**). The derivation shows that the circuit's gain scales the physical collector-base capacitance, C_μ, resulting in the value of the so-called Miller capacitance.

In linear circuits, the Miller term forms a pole by capacitively coupling the stage's output in antiphase to the input. This coupling creates a frequency-dependent negative-feedback term that limits the stage's gain-bandwidth product.

The same physical mechanism affects nonlinear circuits as well. Due to the nature of those circuits' transfer functions, however, the internode capacitive coupling can manifest itself in ways that may not immediately look familiar.

Many high-voltage SMPS (switched-mode-power-supply), motor-drive, and Class-D-amplifier output stages share a common gross topology. This similarity exists despite the diverse parametric requirements these structures must meet.

Though implementations vary, the basic topology is relatively straightforward. A pair of MOSFETs operating as switches alternately connects the output to high- and low-side rails. A timing block generates the control signals that determine the circuit's rms output. The timing controller also ensures that the two switches do not simultaneously conduct by imposing a dead time between the switches' conduction intervals.

The gate-drain capacitance, C_{GD}, is the physical basis for the Miller capacitance in the MOSFET. This parasitic term can affect the behavior of high-voltage switching circuits when the high-side switch turns on to rapidly slew the output node toward the positive rail (**Figure 1**). The positive edge on the low-side FET's drain couples to the gate, and, to the extent that the low-side driver exhibits an ac output impedance, the low-side FET's gate-source voltage, V_{GS}, rises.

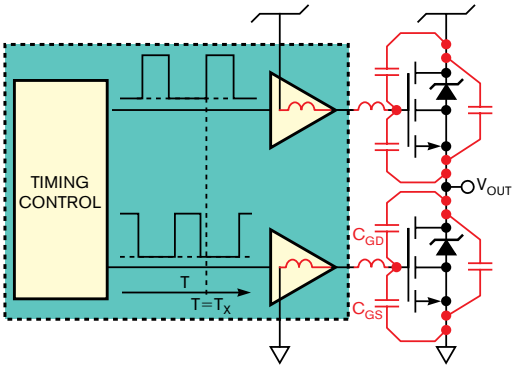

Figure 1 On the rising edge of the output stage, such as at $T=T_X$, the low-side FET can briefly turn on due to a charge that couples through C_{GD}, which degrades the output stage's performance.

If the resultant V_{GS} spike exceeds the device's threshold voltage, V_T, the FET will turn on until its driver can regain control over the gate node. The gate-source capacitance, C_{GS}, mitigates this transient effect, known as CdV/dt turn-on. The transient reduces the operating efficiency of power supplies and motor drives. Audio amplifiers that don't compensate for the output-current error suffer degradation in both harmonic distortion and energy efficiency.

In the limit of driver source impedance and output slew rate, the C_{GS} and C_{GD} terms form a high-frequency voltage divider that attenuates the spike. One of the best ways of preventing CdV/dt turn-on takes advantage of this ac divider.

Power-MOSFET datasheets often carry the typical charge quantities associated with charging the parasitic capacitances to specific voltages. Specifically, Q_{GD} is the charge necessary to raise the C_{GD} parasitic to a specific voltage—often 15V. Q_{GS1} is the charge that the C_{GS} requires to bring the gate to its threshold voltage. To prevent CdV/dt turn-on, a good rule of thumb is to choose a low-side FET with a Q_{GD}-to-Q_{GS1} ratio less than 1.4.

You can minimize the transient turn-on event when it occurs by specifying gate drivers with low output impedances. Also, make sure your product works as well as the paper design by keeping the traces between the driver and the MOSFET gate short. Follow good high-frequency and -current layout practices to minimize stray inductances in the gate-drive loop. EDN

REFERENCE

1 Israelsohn, Joshua, "The Miller's tale," *EDN*, Feb 15, 2007, pg 36, www.edn.com/article/CA6413794.

Contributing Editor Joshua Israelsohn is director, technical information for International Rectifier. Contact him at ednjoshua@sbcglobal.net.